CLAIMS

What is claimed is:

1. A signal scaling circuit, comprising:

a plurality of M switched capacitor circuits operably coupled together;

the M switched capacitor circuits operable to receive a signal from an input source, a reference source and a bias source and further operable to communicate an output signal to an output circuit; and

the M switched capacitor circuits responsive to control circuitry, the control circuitry operable to selectively couple the M switched capacitor circuits to the input source, reference source and bias source such that the output signal communicated to the output circuit includes a portion N/M, where $N < M$, of the input signal.

2. The signal scaling circuit of Claim 1, further comprising the control circuitry operable to selectively couple N switched capacitor circuits to the reference source, the input source and the bias source, as well as M — N switched capacitor circuits to the reference source and the bias source.

3. The signal scaling circuit of Claim 1, further comprising the control circuitry and the M switched capacitor circuits operable to produce an output signal approximating C[reference signal – (N/M)(input signal)], where C is the total capacitance of the M switched capacitor circuits.

4. The signal scaling circuit of Claim 1, further comprising:

the control circuitry operable to divide the M switched capacitor circuits into a first subset of N switched capacitor circuits and a second subset of M — N switched capacitor circuits; and

the first and second switched capacitor circuit subsets operable to substantially simultaneously sample signals selectively coupled thereto.

5. The signal scaling circuit of Claim 4, further comprising the control circuitry operable to alternate the switched capacitor circuits selected for inclusion in the first subset of N switched capacitor circuits and the switched capacitor circuits selected for inclusion in the second subset of M — N switched capacitor circuits.

6. The signal scaling circuit of Claim 1, wherein each of the plurality of M switched capacitor circuits comprise two capacitors.

7. The signal scaling circuit of Claim 1, further comprising the output circuit including an inverting integrator having at least one feedback capacitor.

8. The signal scaling circuit of Claim 1, further comprising the input, reference and bias sources coupled to the M switched capacitor circuits in accordance with a differential topology.

9. A circuit for generating at an output node an output signal including a scale factor N/M of an input signal, the circuit comprising:

an input node operable to receive an input signal from an input signal source;

a reference node operable to receive a reference signal from a reference signal source;

a bias node operable to receive a bias signal from a bias signal source;

M switched capacitor circuits selectively coupled to the input signal node, reference node, bias node and output node; and

control circuitry coupled to the M switched capacitor circuits, the control circuitry and the M switched capacitor circuits cooperating to create a first subset of N switched capacitor circuits and a second subset of M — N switched capacitor circuits and wherein the N switched capacitor circuits selectively sample the reference signal and the input signal and the M — N switched capacitor circuits selectively sample the reference signal such that the output signal at the output node includes the scale factor N/M of the input signal.

10. The circuit of Claim 9, further comprising the first subset and the second subset of switched capacitor circuits cooperating to produce an output signal at the output node including a scale factor N/M of the input signal, where $N < M$.

11. The circuit of Claim 9, further comprising at least one of the signal sources coupled to common mode voltage source (V_{CM}).

12. The circuit of Claim 9, further comprising the bias signal source including an offset component.

13. The circuit of Claim 9, further comprising the control circuitry and the M switched capacitor circuits cooperating to alternate the switched capacitor circuits populating the first and second switched capacitor circuit subsets.

14. The circuit of Claim 9, further comprising:

the M switched capacitor circuits having a total capacitance of C; and

each of the M switched capacitor circuits having a capacitance substantially equal to C/M.

15. The circuit of Claim 14, further comprising the control circuitry and the M switched capacitors cooperating to produce at the output node an output signal approximating C[reference signal – (N/M)(input signal)].

16. A signal processing apparatus, comprising:

an input node operable to receive an input signal;

a reference node operable to receive a reference signal;

a bias node operable to receive a bias signal;

an output node operable to communicate an output signal to an output circuit;

a plurality of M switched capacitor circuits operably coupled to the input node, reference node, bias node and output node, each switched capacitor having substantially equivalent capacitance C/M; and

control circuitry operably coupled to the M switched capacitor circuits, the control circuitry operable to divide the M switched capacitor circuits into a subset of

N switched capacitor circuits and a subset of M — N switched capacitor circuits and to cause each of the N switched capacitor circuits to deliver a signal approximating (C/M)(reference signal — input signal) and each of the M — N switched capacitor circuits to deliver a signal approximating (C/M)(reference signal) to the output node.

17. The signal processing apparatus of Claim 16, further comprising the M switched capacitors and the control circuitry cooperating to produce an output signal including a portion N/M of the input signal.

18. The signal processing apparatus of Claim 16, further comprising the control circuitry cooperating with the M switched capacitor circuits to alternate the switched capacitor circuits included in the subset of N switched capacitor circuits and the subset of M — N switched capacitor circuits.

19. The signal processing apparatus of Claim 18, further comprising alternating the switched capacitor circuits in N and M — N switched capacitor circuit subsets in successive clock periods.

20. A method of scaling an input signal, comprising:

from a set of M switched capacitor circuits, selectively coupling a first and a second subset of switched capacitor circuits to an input source, a reference source and a bias source; and

communicating an output signal including a scale factor N/M of the input signal to an output node in each clock cycle.